For Quartus® Prime 15.0 and 15.1, update the Quartus Prime Settings File (.qsf) with the below settings for your PCIe design that targets an Arria® 10 ES2, ES3 or production device.

In the following, "_N" represents the lane and you must have one set of these constraints per lane. For example if you have a two lane design, then you would have a set of constraints for lane 0 (N=0, e.g. "txrx_rx_data_0") and another set for lane 1 (N=1, e.g. "txrx_rx_data_1"). Note that there are separate transceiver transmit and receive constraints.

set_instance_assignment -name XCVR_A10_RX_TERM_SEL R_R1 -to <txvr_rx_data_pin_N>
set_instance_assignment -name XCVR_A10_RX_ONE_STAGE_ENABLE NON_S1_MODE -to <txvr_rx_data_pin_N>
set_instance_assignment -name XCVR_A10_RX_ADP_CTLE_ACGAIN_4S RADP_CTLE_ACGAIN_4S_7 -to <txrx_rx_data_pin_N>
set_instance_assignment -name XCVR_A10_RX_EQ_DC_GAIN_TRIM STG1_GAIN7 -to <txvr_rx_data_pin_N>
set_instance_assignment -name XCVR_A10_RX_ADP_VGA_SEL RADP_VGA_SEL_4 -to <txvr_rx_data_pin_N>
set_instance_assignment -name XCVR_VCCR_VCCT_VOLTAGE 1_0V -to <txvr_rx_data_pin_N>
set_instance_assignment -name XCVR_VCCR_VCCT_VOLTAGE 1_0V -to <txvr_tx_data_pin_N>

You must also drive the corresponding transceiver power pins of your PCIe IP core with 1.03 V.